

**SPECIFICATION
FOR
LCM Module**

MODULE No:	KD043WVFIA083
CUSTOMER:	

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Part. No	KD043WVFIA083	REV	V1.0	Page 1 of 31
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常备库存
Stock For Sale

长期供货
Long Time supply

支持小量
NO MOQ

品种齐全
In Full Range

Contents

1.	Block Diagram	5
2.	Outline dimension	6
3.	Input terminal Pin Assignment	7
4.	LCD Optical Characteristics	8
4.1	Optical specification	错误!未定义书签。
5.	TFT Electrical Characteristics	错误!未定义书签。
5.1	Absolute Maximum Rating (Ta=25 VSS=0V).....	错误!未定义书签。
5.2	DC Electrical Characteristics.....	错误!未定义书签。
5.3	LED Backlight Characteristics	错误!未定义书签。
6.	MIPI Interface Characteristics	11
6.1	High Speed Mode – Clock Channel Timing.....	14
6.2	High Speed Mode – Data Clock Channel Timing	15
6.3	High Speed Mode – Rising and Fall Timings	16
6.4	Low Speed Mode – Bus Turn Around.....	17
6.5	Data Lanes from Low Power Mode to High Speed Mode	18
6.6	Data Lanes from High Power Mode to High Speed Mode.....	19
6.7	DSI Clock Burst – High Speed Mode to/from Low Power Mode.....	20
6.8	Timing for DSI video mode.....	21
6.9	Reset input timing	21
7.	LCD Module Out-Going Quality Level	错误!未定义书签。
7.1	VISUAL & FUNCTION INSPECTION STANDARD	错误!未定义书签。
7.1.1	Inspection conditions	错误!未定义书签。
7.1.2	Definition	错误!未定义书签。
7.1.3	Sampling Plan	错误!未定义书签。
7.1.4	Criteria (Visual).....	错误!未定义书签。
8.	Reliability Test Result	错误!未定义书签。
9.	Cautions and Handling Precautions	错误!未定义书签。
9.1	Handling and Operating the Module.....	错误!未定义书签。
9.2	Storage and Transportation.....	错误!未定义书签。
10.	Packing.....	错误!未定义书签。

Part. No	KD043WVFIA083	REV	V1.0	Page 3 of 31
常备库存 Stock For Sale	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range	

*** Description**

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 4.3'TFT-LCD contains 480x800 pixels, and can display up to 65K/262K/16.7M colors.

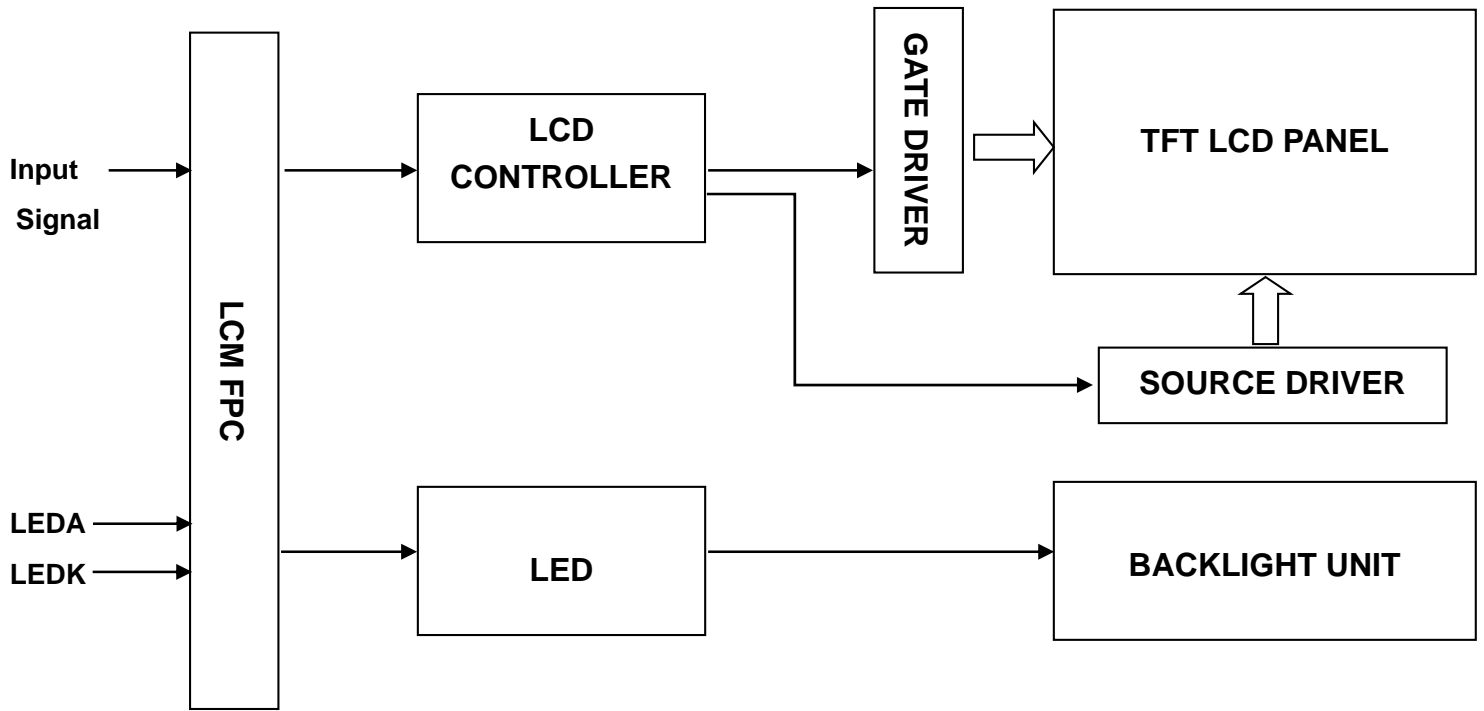
*** Features**

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	56.16(H)*93.60(V) (4.3inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	16.7M	colors	-
Number of pixels	480(RGB)*800	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.117(H)*0.117(V)	mm	-
Viewing angle	ALL	o'clock	-
TFT Controller IC	ILI9806E	-	-
Display mode	Transmissive/Normally Black	-	-
Operating temperature	-20~+70	°C	-
Storage temperature	-30~+80	°C	-

*** Mechanical Information**

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		62.50		mm	-
	Vertical(V)		105.55		mm	-
	Depth(D)		2.65		mm	-
Weight			TBD		g	-

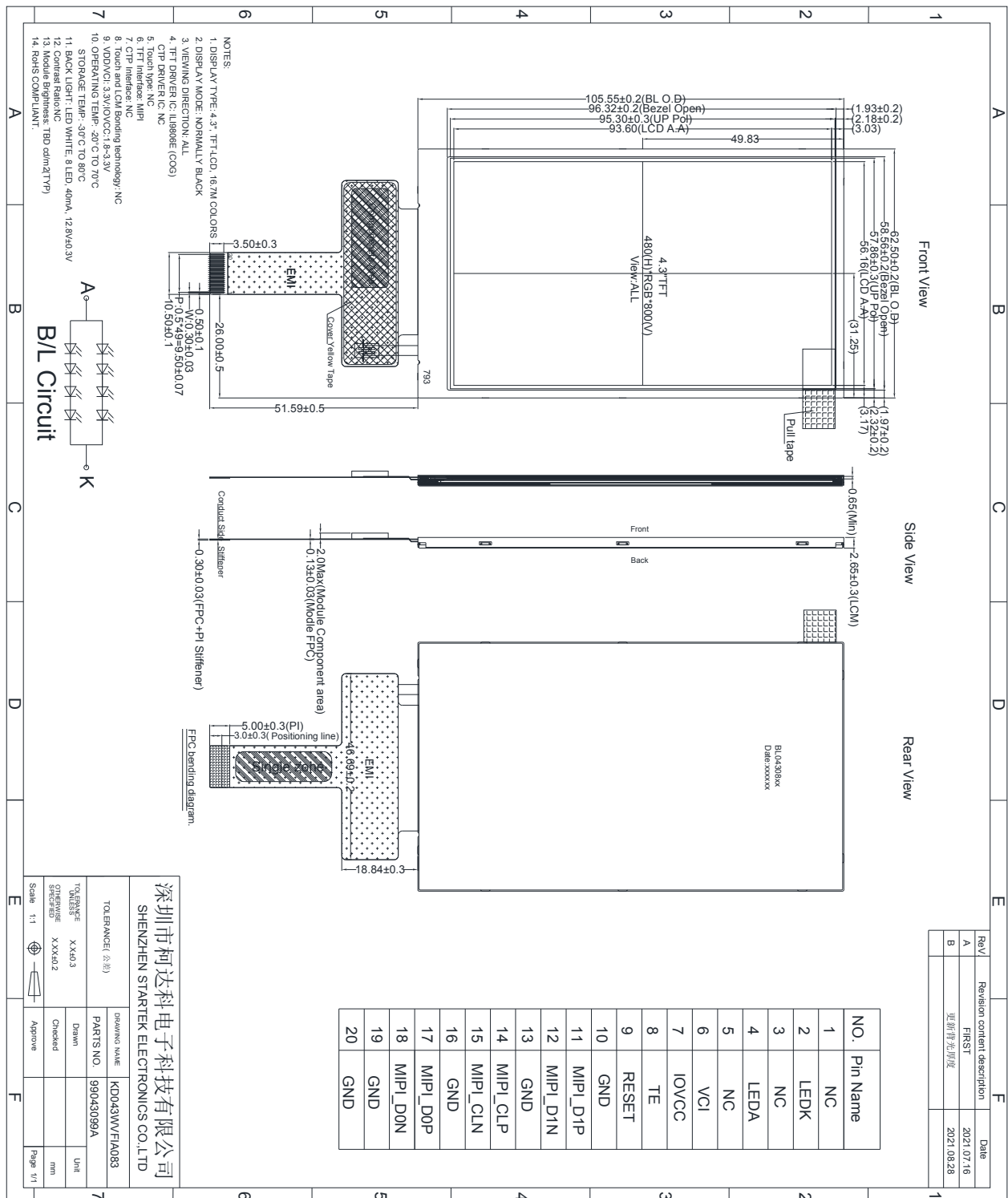
1. Block Diagram



Part. No	KD043WVFIA083	REV	V1.0	Page 5 of 31
常备库存 Stock For Sale	长期供货 Long Time supply		支持小量 NO MOQ	品种齐全 In Full Range



2. Outline dimension



Part. No	KD043WV/FIA083	REV	V1.0	Page 6 of 31
常备库存 Stock For Sale	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range	

3. Input terminal Pin Assignment

NO.	SYMBOL	DISCRIPTION	I/O
1	NC		
2	LEDK	Cathode pin of backlight.	P
3	NC		
4	LEDA	Anode pin of backlight.	P
5	NC		
6	VCI	Supply Voltage (3.3V).	P
7	IOVCC	I/O power supply voltage.	P
8	TE	-Tearing effect output Leave the pin to open when not in use.	O
9	RESET	- The external reset input. Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.	I
10	GND	Ground.	P
11	MIPI_D1P	MIPI DSI differential data pair (DSI-Dn+/-).	I/O
12	MIPI_D1N	If MIPI are not used, they should be connected to DGND	I/O
13	GND	Ground.	P
14	MIPI_CLP	MIPI DSI differential clock pair (DSI-CLK+/-).	I
15	MIPI_CLN	If MIPI are not used, they should be connected to DGND.	I
16	GND	Ground.	P
17	MIPI_D0P	MIPI DSI differential data pair (DSI-Dn+/-).	I/O
18	MIPI_D0N	If MIPI are not used, they should be connected to DGND	I/O
19	GND	Ground.	P
20	GND	Ground.	P

4. LCD Optical Characteristics

4.1 Optical specification

Item	Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio	CR		1000	1300	--		(1)(2)
Response time	Rising	T_R	--	35	40	msec	(1)(3)
	Falling	T_F					
Color gamut	S(%)		59	64	--	%	
Color Filter Chromaticity	White	W_X	$\Theta=0$ Normal viewing angle	0.2746	0.3146	0.3546	(1)(4) CA-310
		W_Y		0.3208	0.3608	0.4008	
	Red	R_X		0.5956	0.6356	0.6756	
		R_Y		0.3113	0.3513	0.3913	
	Green	G_X		0.2720	0.3120	0.3520	
		G_Y		0.5324	0.5724	0.6124	
	Blue	B_X		0.1042	0.1442	0.1842	
		B_Y		0.0219	0.0619	0.0659	
Viewing angle	Hor.	Θ_L	CR>10	70	80	--	(1)(4)
		Θ_R		70	80	--	
	Ver.	Θ_U		70	80	--	
		Θ_D		70	80	--	
Option View Direction	ALL						

*The data comes from the LCD specification.

Measuring Condition

Measuring surrounding : dark room

Ambient temperature : $25 \pm 2^\circ\text{C}$

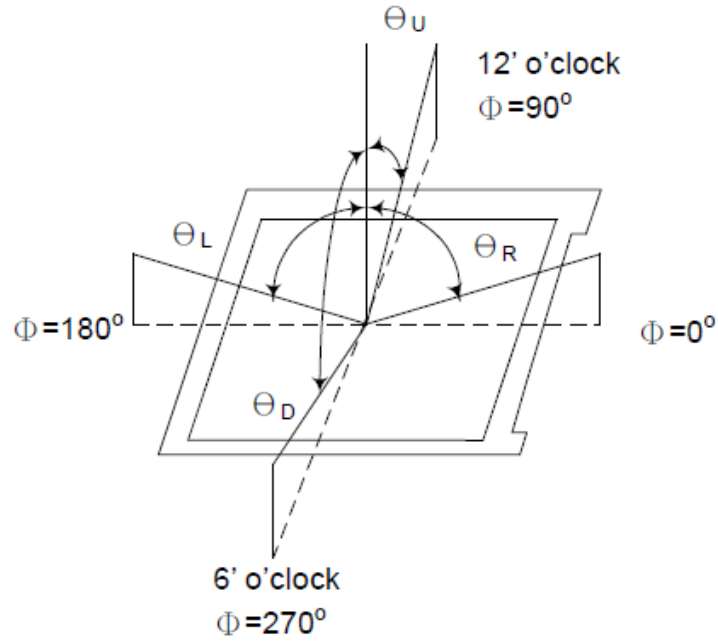
15min. warm-up time.

Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

Note (1): Definition of Viewing Angle :

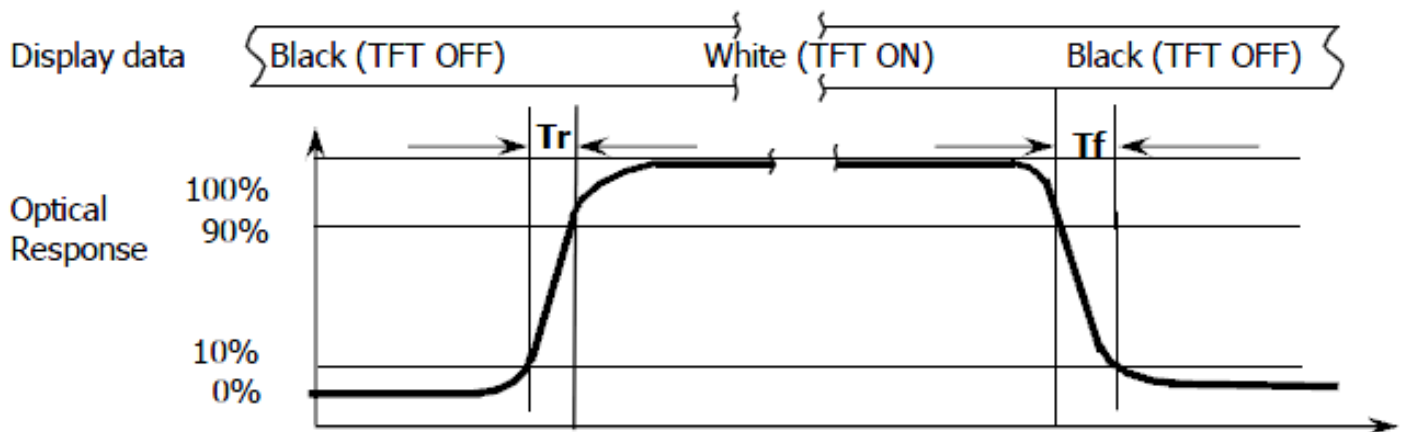
Part. No	KD043WVFIA083	REV	V1.0	Page 8 of 31
常备库存 Stock For Sale	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range	



Note (2): Definition of Contrast Ratio(CR) :measured at the center point of panel

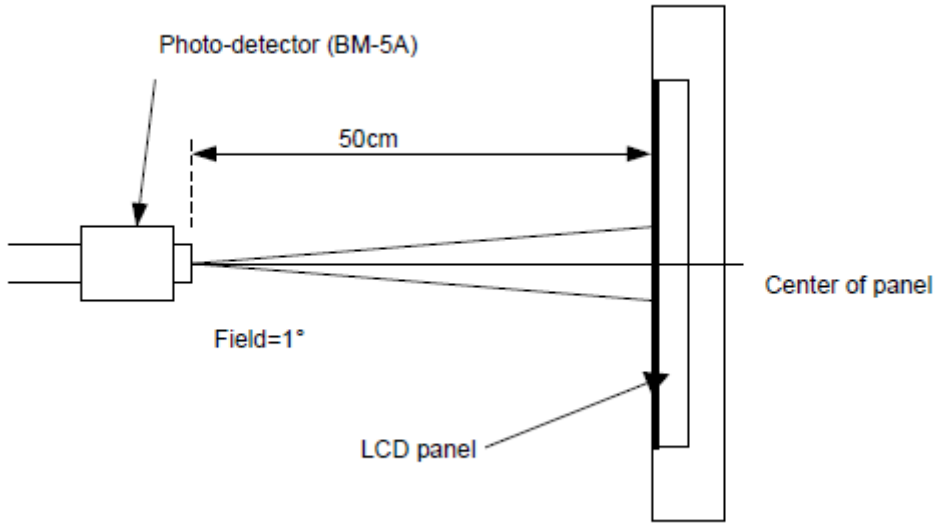
$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3): Response Time



Note (4): Definition of optical measurement setup

Part. No	KD043WVFIA083	REV	V1.0	Page 9 of 31
常备库存 Stock For Sale	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range	



Part. No	KD043WVFIA083	REV	V1.0	Page 10 of 31
常备库存 Stock For Sale	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range	

5. Electrical Characteristics

5.1 Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	V _{CI}	-0.3	4.6	V	Note1
Digital Interface Supply Voltage	V _{DDIO}	-0.3	4.6		
Operating temperature	T _{OP}	-20	+70	°C	
Storage temperature	T _{ST}	-30	+80	°C	

NOTE1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	V _{CI}	2.5	3.3	3.6	V	
Digital interface supple Voltage	V _{DDIO}	1.65	1.8	3.6		
Normal mode Current	I _{CC}	--	30	60	mA	
Level input voltage	V _{IH}	0.7* V _{DDIO}	--	V _{DDIO}	V	
	V _{IL}	GND	--	0.3* V _{DDIO}	V	
Level output voltage	V _{OH}	0.8*V _{DDIO}	--	V _{DDIO}	V	
	V _{OL}	GND	--	0.2*V _{DDIO}	V	

5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 8 chips LED

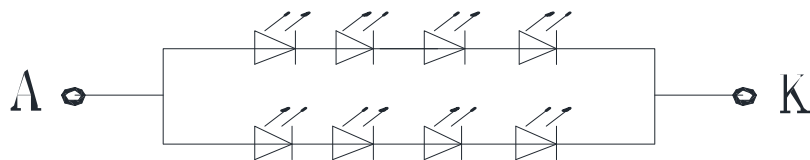
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	35	40	--	mA	
Forward Voltage	V_F	--	12.8	--	V	
LCM Luminance ($I_F = 20\text{mA}$)	LV	400	450	--	cd/m ²	Note3
LED life time	Hr	50000	--	--	Hour	Note1,2
Uniformity	Avg	80	--	--	%	Note3

Note1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition:

$T_a = 25 \pm 3 \text{ } ^\circ\text{C}$, typical IL value indicated in the above table until the brightness becomes less than 50%.

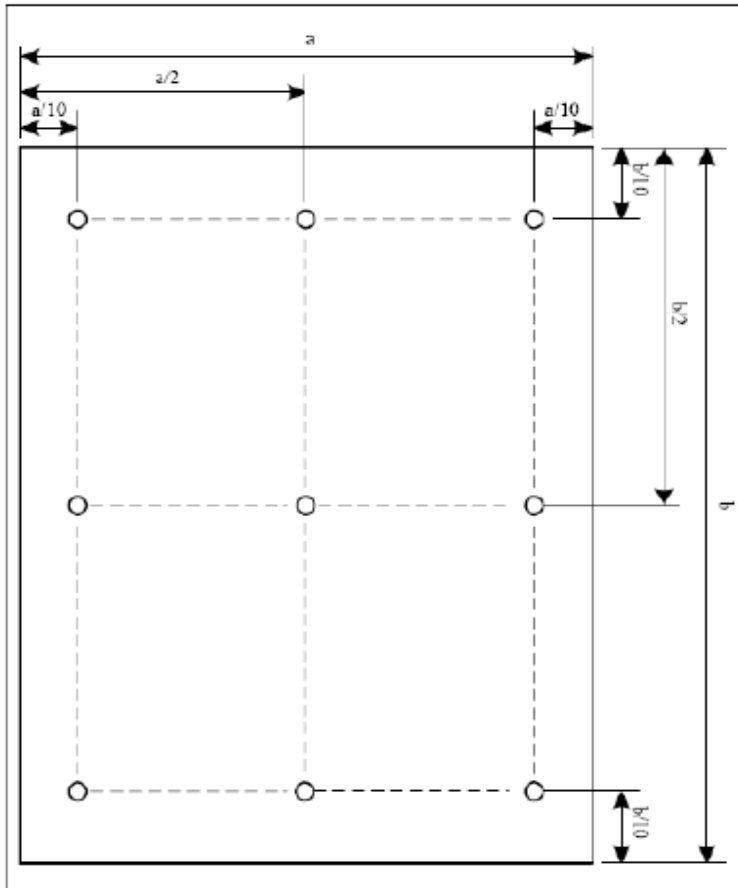
Note 2: The "LED life time" is defined as the module brightness decrease to 50% original brightness at $T_a = 25 \text{ } ^\circ\text{C}$

and $I_L = 40\text{mA}$. The LED lifetime could be decreased if operating I_L is larger than 40mA. The constant current driving method is suggested.



B/L Circuit

Note (3) Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

Part. No	KD043WVFIA083	REV	V1.0	Page 13 of 31
常备库存 Stock For Sale	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range	

6. MIPI Interface Characteristics

6.1 High Speed Mode – Clock Channel Timing

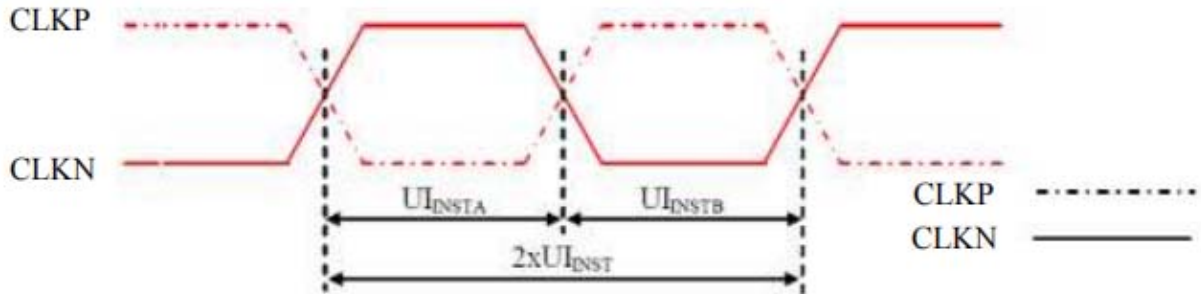


Figure 116: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	Note 2	25	ns
CLKP/N	UI_{INSTA}, UI_{INSTB} (Note 1)	UI instantaneous Half	Note 2	12.5	ns

Notes:

1. $UI = UI_{INSTA} = UI_{INSTB}$
2. Define the minimum value, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	466 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	525 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps

Part. No	KD043WVFIA083	REV	V1.0	Page 14 of 31
常备库存 Stock For Sale	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range	

6.2 High Speed Mode – Data Clock Channel Timing

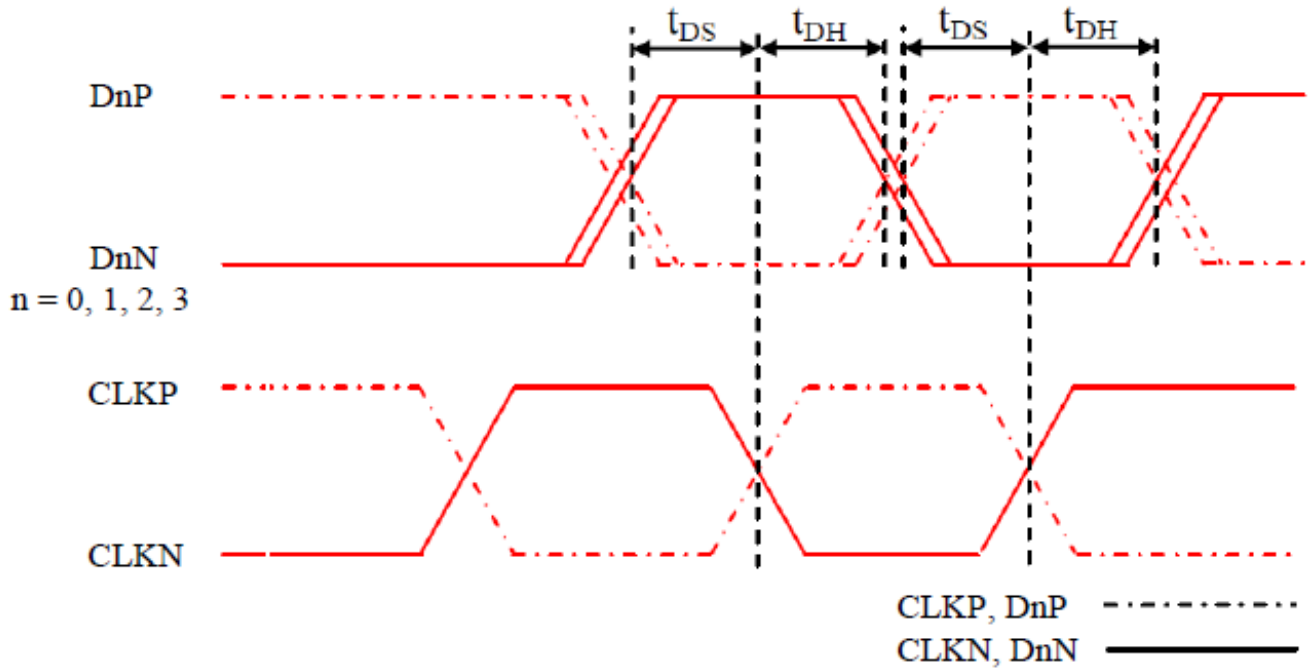


Figure 119: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

6.3 High Speed Mode – Rising and Fall Timings

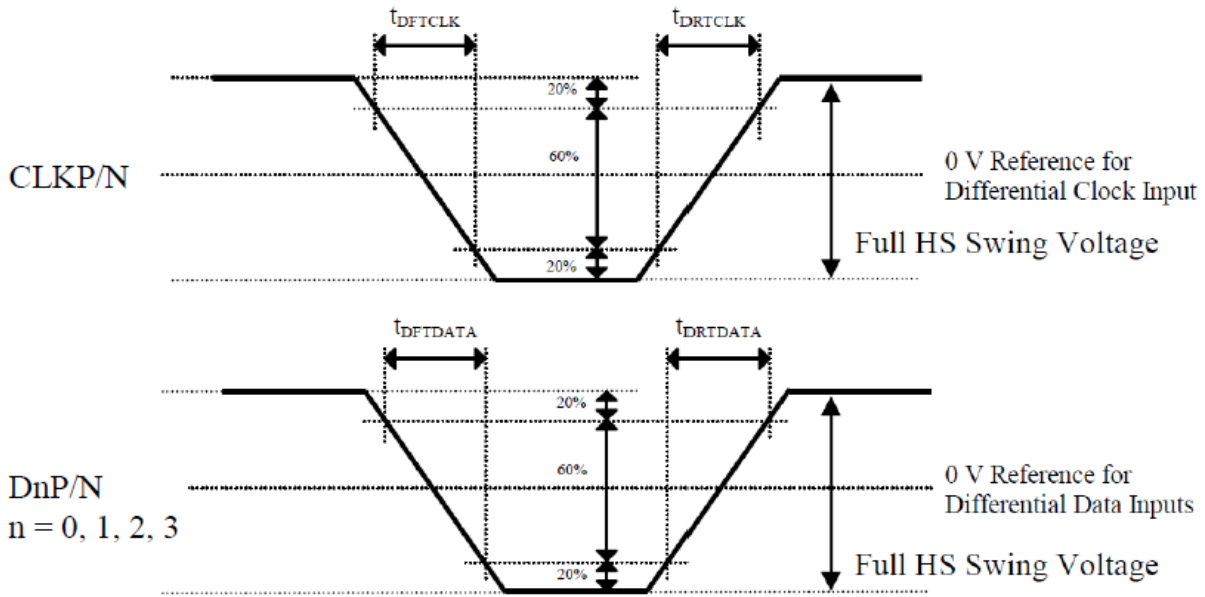


Figure 120: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.

6.4 Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C) are illustrated for reference purposes below.

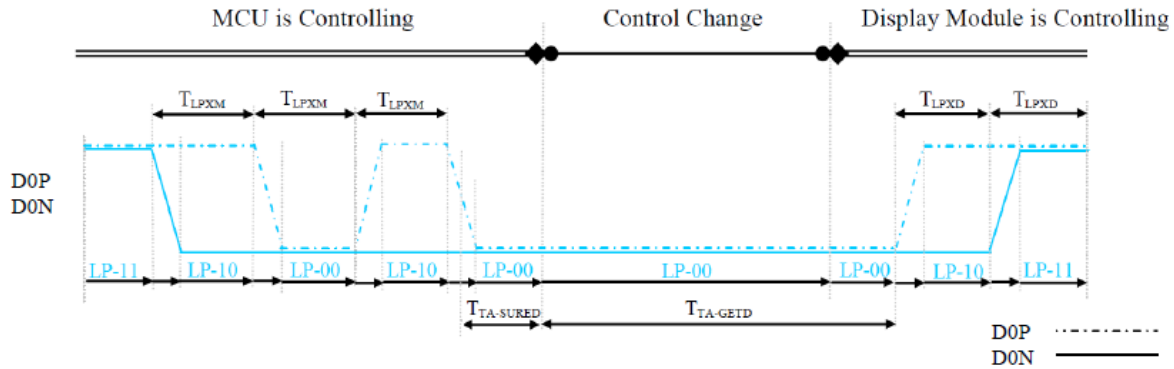


Figure 121: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C) to the MCU are illustrated for reference purposes below.

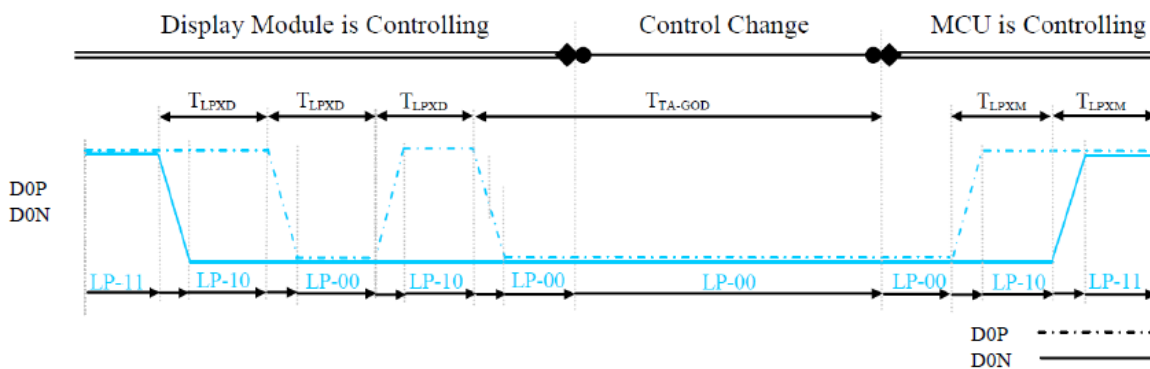


Figure 122: BTA from the Display Module to the MCU

Table 42: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → Display Module (ILI9881C)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C) → MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C) starts driving	T_{LPXD}	$2 \times T_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C)	$5 \times T_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4 \times T_{LPXD}$	ns

Part. No	KD043WVFIA083	REV	V1.0	Page 17 of 31
常备库存 Stock For Sale	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range	

6.5 Data Lanes from Low Power Mode to High Speed Mode

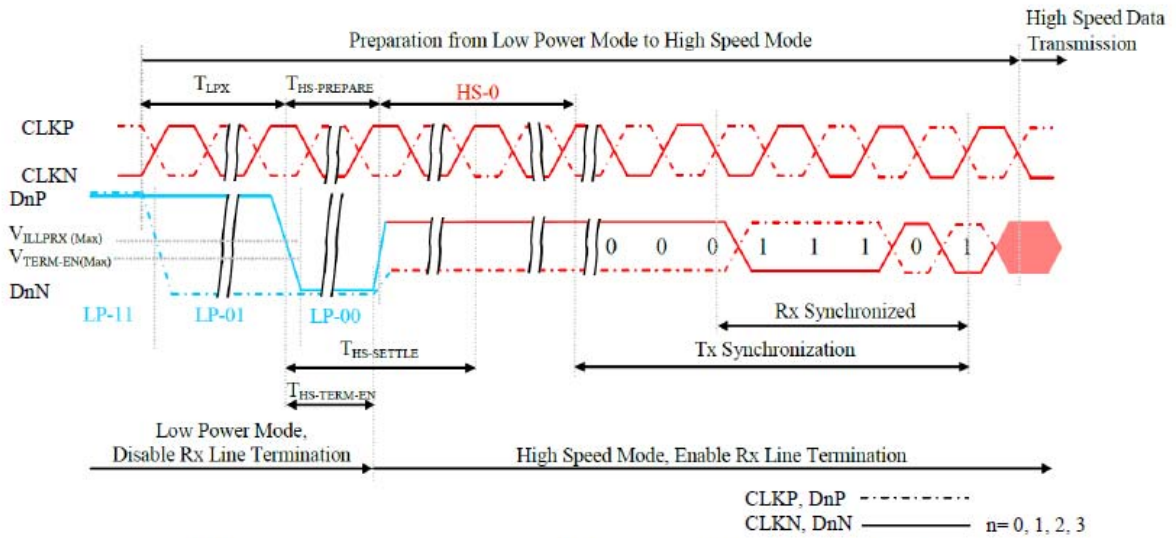


Figure 123: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	$40+4xUI$	$85+6xUI$	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	$35+4xUI$	ns

Part. No	KD043WVFIA083	REV	V1.0	Page 18 of 31
常备库存 Stock For Sale	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range	

6.6 Data Lanes from High Power Mode to High Speed Mode

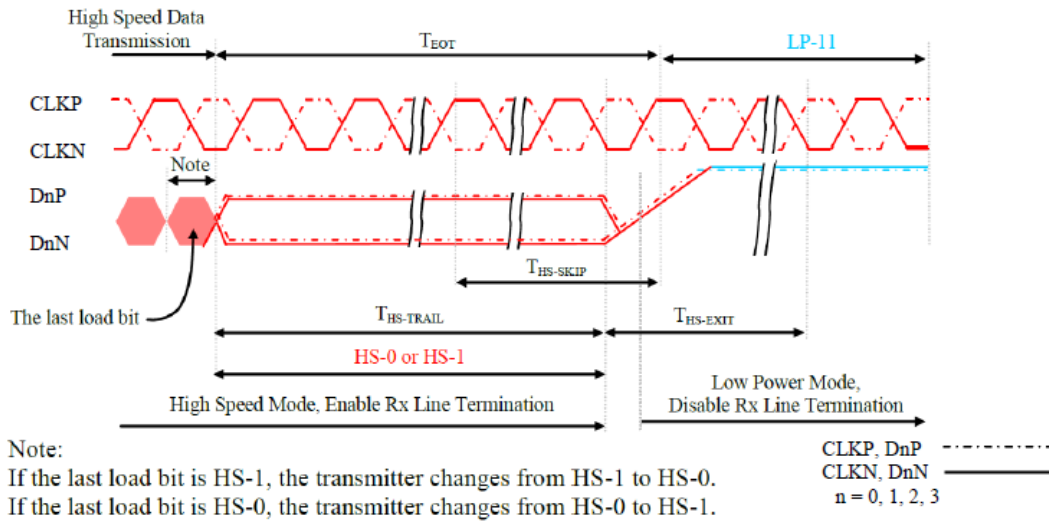


Figure 124: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C) to ignore transition period of EoT	40	$55+4 \times UI$	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

6.7 DSI Clock Burst – High Speed Mode to/from Low Power Mode

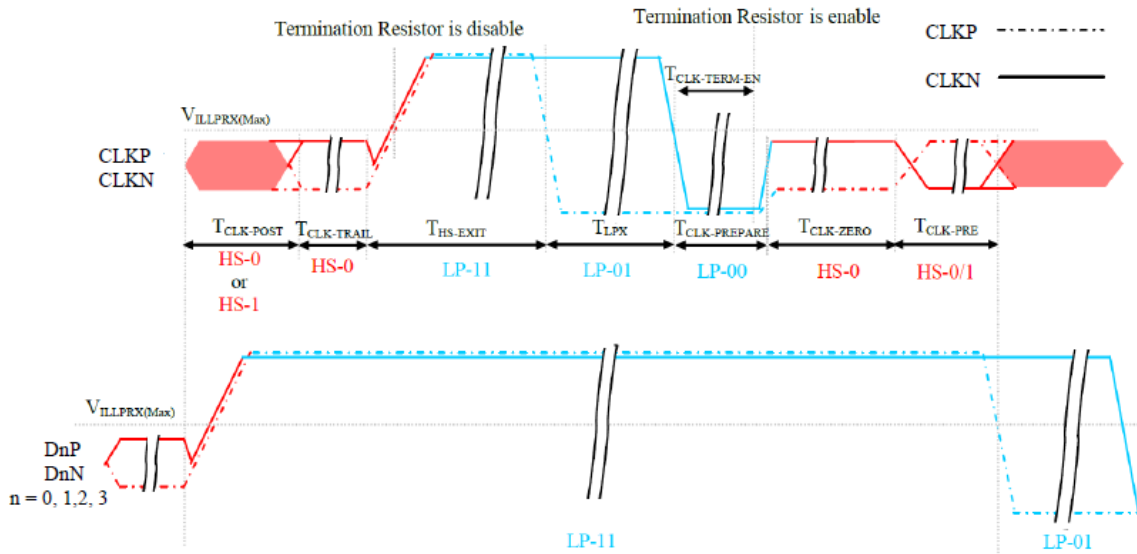


Figure 125: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	$60+52xUI$	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	$8xUI$	-	ns

6.8 Timing for DSI video mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
DCLK frequency	FCLK	--	(67)	--	MHz
Horizontal display area	HDISP	--	800	--	Clock
Horizontal Sync. Width	hpw	1	4	--	Clock
Horizontal Sync. Back Porch	hbp	1	38	-	Clock
Horizontal Sync. Front Porch	hfp	1	16	--	Clock
Vertical display area	VDISP	--	1280	--	Line
Vertical Sync. Width	vs	1	4	--	Line
Vertical Sync. Back Porch	vbp	1	10	--	Line
Vertical Sync. Front Porch	vfp	1	8	--	Line
Frame-Rate		--	60	--	Hz

Note:s

The best frame rate setting : 2 data lanes : 50~60 Hz / 3 data lanes : 50~70 Hz / 4 data lanes : 50~70 Hz.

6.9 Reset input timing

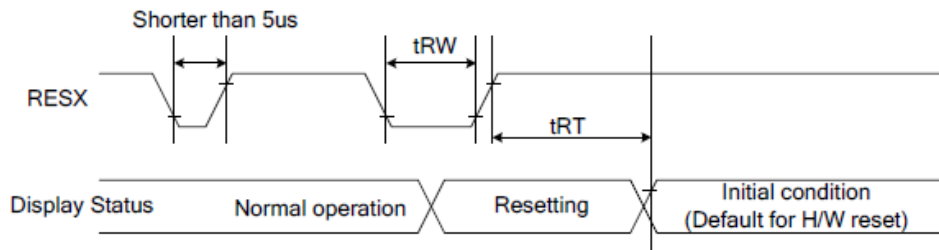


Figure 126: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5) 120 (note 1,6,7)	mS

Notes:

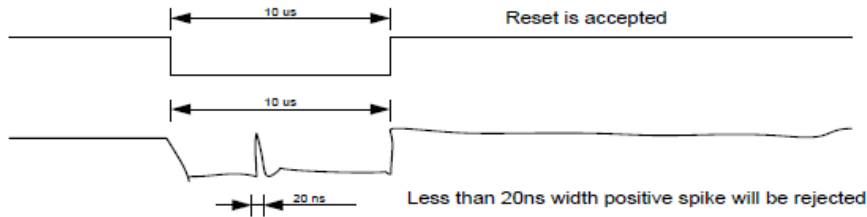
1. The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.

Part. No	KD043WVFIA083	REV	V1.0	Page 21 of 31
常备库存 Stock For Sale	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range	

Table 48: Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

- During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
- Spike Rejection can also be applied during a valid reset pulse, as shown below:


Figure 127: Positive Noise Pulse during Reset Low

- When Reset applied during Sleep In Mode.
- When Reset applied during Sleep Out Mode.
- It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7. LCD Module Out-Going Quality Level

7.1 VISUAL & FUNCTION INSPECTION STANDARD

7.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

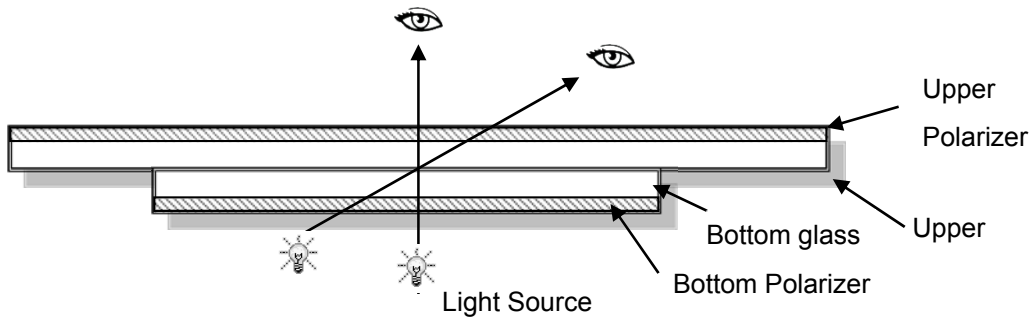
Temperature : 25±5℃

Humidity : 65%±10%RH

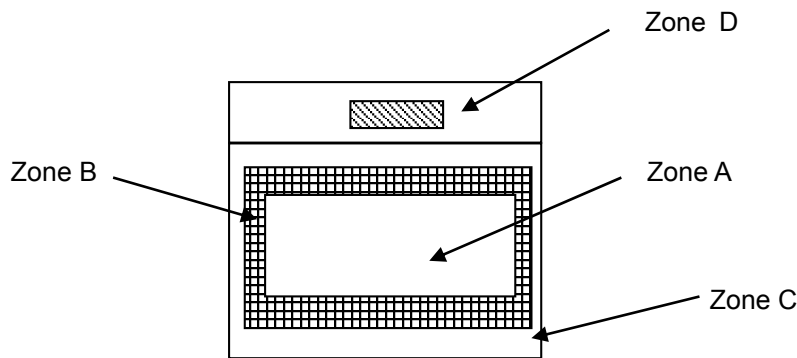
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



7.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer

Zone D : IC Bonding Area

Note:As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

Part. No	KD043WVFIA083	REV	V1.0	Page 23 of 31
常备库存 Stock For Sale	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range	

7.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

AQL:

Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , LCM: Liquid Crystal Module,

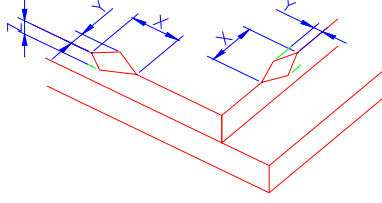
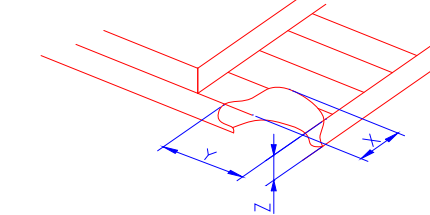
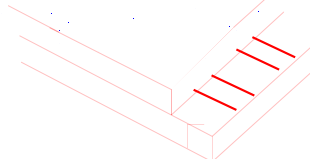
No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. etc...	Major
2	Missing	Missing components and etc...	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed, deformation and etc...	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot/Line defect	Light dot, Dim spot, (Note1) Polarizer Air Bubble, Polarizer accidented spot and etc.	
6	Soldering appearance	Good soldering , Peeling off is not allowed and etc.	
7	LCD/Polarizer	Black/White spot/line, scratch, crack, etc.	

Note1: a) Light dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.



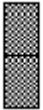
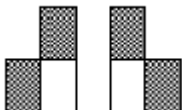
Part. No	KD043WVFIA083	REV	V1.0	Page 24 of 31
常备库存 Stock For Sale	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range	

7.1.4 Criteria (Visual)


Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken NOTE: X: Length Y: Width Z: Height L: Length of ITO, T: Height of LCD	(1) The edge of LCD broken	 <table border="1" data-bbox="758 672 1452 817"> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>≤3.0mm</td> <td><Inner border line of the seal</td> <td>≤T</td> </tr> </tbody> </table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
X	Y	Z						
≤3.0mm	<Inner border line of the seal	≤T						
	(2)LCD corner broken	 <table border="1" data-bbox="837 1131 1372 1220"> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>≤3.0mm</td> <td>≤L</td> <td>≤T</td> </tr> </tbody> </table>	X	Y	Z	≤3.0mm	≤L	≤T
X	Y	Z						
≤3.0mm	≤L	≤T						
	(3) LCD crack	 <p style="text-align: center;">Crack Not allowed</p>						



2.0	Spot defect	① light dot (black/white spot , pinhole, stain, etc.)			
	<p>$\Phi=(X+Y)/2$</p>	Acceptable Qty			
		Zone	A	B	C
		Size (mm)	Ignore		
$\Phi \leq 0.15$		Ignore			
	$0.15 < \Phi \leq 0.25$	3(distance ≥ 10 mm)			
	$0.25 < \Phi \leq 0.4$	2(distance ≥ 10 mm)			
	$\Phi > 0.4$	0			
		② Dim spot (light leakage、dent、dark spot, etc)			
		Acceptable Qty			
	Zone	A	B	C	
	Size (mm)	Ignore			
	$\Phi \leq 0.15$	Ignore			
	$0.15 < \Phi \leq 0.25$	3(distance ≥ 10 mm)			
	$0.25 < \Phi \leq 0.4$	2(distance ≥ 10 mm)			
	$\Phi > 0.4$	0			
		③ Polarizer accidented spot			
		Acceptable Qty			
	Zone	A	B	C	
	Size (mm)	Ignore			
	$\Phi \leq 0.2$	Ignore			
	$0.2 < \Phi \leq 0.5$	2(distance ≥ 10 mm)			
	$\Phi > 0.5$	0			
		④Polarizer Bubble			
		Acceptable Qty			
	Zone	A	B	C	
	Size (mm)	Ignore			
	$\Phi \leq 0.2$	Ignore			
	$0.2 < \Phi \leq 0.4$	3(distance ≥ 10 mm)			
	$\Phi > 0.4$	0			

3.0	LCD Pixel defect	<p>Pixel bad points</p> <table border="1"> <thead> <tr> <th data-bbox="539 309 730 360">Item</th> <th data-bbox="730 309 1246 360">Zone A</th> <th data-bbox="1246 309 1497 360">Acceptable Qty</th> </tr> </thead> <tbody> <tr> <td data-bbox="539 360 730 521" rowspan="3">Bright dot</td> <td data-bbox="730 360 1246 416">Random</td> <td data-bbox="1246 360 1497 416">N≤2</td> </tr> <tr> <td data-bbox="730 416 1246 472">2 dots adjacent</td> <td data-bbox="1246 416 1497 472">N≤0</td> </tr> <tr> <td data-bbox="730 472 1246 521">3 dots adjacent</td> <td data-bbox="1246 472 1497 521">N≤0</td> </tr> <tr> <td data-bbox="539 521 730 692" rowspan="3">Dark dot</td> <td data-bbox="730 521 1246 577">Random</td> <td data-bbox="1246 521 1497 577">N≤2</td> </tr> <tr> <td data-bbox="730 577 1246 633">2 dots adjacent</td> <td data-bbox="1246 577 1497 633">N≤0</td> </tr> <tr> <td data-bbox="730 633 1246 692">3 dots adjacent</td> <td data-bbox="1246 633 1497 692">N≤0</td> </tr> <tr> <td data-bbox="539 692 730 1003">Distance</td> <td data-bbox="730 692 1246 1003"> 1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot. </td> <td data-bbox="1246 692 1497 1003">5mm</td> </tr> <tr> <td colspan="2" data-bbox="539 1003 1246 1059">Total bright and dark dot</td> <td data-bbox="1246 1003 1497 1059">N≤4</td> </tr> </tbody> </table> <p>Note:</p> <p>A) Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.</p> <p>B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.</p> <p>C) 2 dot adjacent = 1 pair = 2 dots</p> <p>Picture:</p> <div style="display: flex; justify-content: space-around; align-items: flex-start;"> <div style="text-align: center;">  <p>2 dot adjacent</p> </div> <div style="text-align: center;">  <p>2 dot adjacent</p> </div> </div> <div style="display: flex; justify-content: space-around; align-items: flex-start; margin-top: 20px;"> <div style="text-align: center;">  <p>2 dot adjacent (vertical)</p> </div> <div style="text-align: center;">  <p>2 dot adjacent (slant)</p> </div> </div>	Item	Zone A	Acceptable Qty	Bright dot	Random	N≤2	2 dots adjacent	N≤0	3 dots adjacent	N≤0	Dark dot	Random	N≤2	2 dots adjacent	N≤0	3 dots adjacent	N≤0	Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm	Total bright and dark dot		N≤4
Item	Zone A	Acceptable Qty																							
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	3 dots adjacent	N≤0																							
Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm																							
Total bright and dark dot		N≤4																							



4.0	Line defect (LCD /Polarizer backlight black/white line, scratch, stain)  W: width, L : length N : Count	<table border="1"> <thead> <tr> <th rowspan="2">Width(mm)</th> <th rowspan="2">Length(m)</th> <th colspan="3">Acceptable Qty</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.05$</td> <td>Ignore</td> <td colspan="2">Ignore</td> <td rowspan="3">Ignore</td> </tr> <tr> <td>$0.05 < W \leq 0.06$</td> <td>$L \leq 4.0$</td> <td colspan="2">$N \leq 3$</td> </tr> <tr> <td>$0.06 < W \leq 0.08$</td> <td>$L \leq 3.0$</td> <td colspan="2">$N \leq 2$</td> </tr> <tr> <td>$W > 0.08$</td> <td colspan="4">Define as spot defect</td> </tr> </tbody> </table>	Width(mm)	Length(m)	Acceptable Qty			A	B	C	$\Phi \leq 0.05$	Ignore	Ignore		Ignore	$0.05 < W \leq 0.06$	$L \leq 4.0$	$N \leq 3$		$0.06 < W \leq 0.08$	$L \leq 3.0$	$N \leq 2$		$W > 0.08$	Define as spot defect			
		Width(mm)			Length(m)	Acceptable Qty																						
			A	B		C																						
		$\Phi \leq 0.05$	Ignore	Ignore		Ignore																						
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$0.06 < W \leq 0.08$	$L \leq 3.0$	$N \leq 2$																										
$W > 0.08$	Define as spot defect																											
5.0	Electronic Components SMT.	Not allow missing parts, solderless connection, cold solder joint, mismatch. The positive and negative polarity opposite																										
6.0	Display color & Brightness.	1. Color: Measuring the color coordinates, The measurement standard according to the datasheet or samples. 2. Brightness: Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.																										
7.0	LCD Mura/Waving/ Hot spot	Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.																										

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed

8. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	70℃,96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operating	-20℃, 96HR	
High Temperature Storage	80℃, 96HR	
Low Temperature Storage	-30℃, 96HR	
High Temperature & High Humidity Operating	+60℃, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-10℃,30 min ↔ 60℃,30 min, Change time:5min 20CYC.	
ESD test	C=150pF, R=330,5points/panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15℃~35℃, 30%~60%).	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80cm(MEDIUM BOX)	

Remark:

- 1.The test samples should be applied to only one test item.
- 2.Sample size for each test item is 5~10pcs.
- 3.For Damp Proof Test, Pure water(Resistance > 10MΩ) should be used.
- 4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
- 5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
6. The color fading mura of polarizing filter should not care.

Part. No	KD043WVFIA083	REV	V1.0	Page 29 of 31
常备库存 Stock For Sale	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range	

9. Cautions and Handling Precautions

9.1 Handling and Operating the Module

- (1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
- (2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
- (3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
- (4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
- (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static; it may cause damage to the CMOS ICs.
- (9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (10) Do not disassemble the module.
- (11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (12) Pins of I/F connector shall not be touched directly with bare hands.
- (13) Do not connect, disconnect the module in the "Power ON" condition.
- (14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

9.2 Storage and Transportation.

- (1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%
- (2) Do not store the TFT-LCD module in direct sunlight.
- (3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
- (4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
- (5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed

Part. No	KD043WVFIA083	REV	V1.0	Page 30 of 31
常备库存 Stock For Sale	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range	

10. Packing

----TBD-----

Part. No	KD043WVFIA083	REV	V1.0	Page 31 of 31
	常备库存 Stock For Sale	长期供货 Long Time supply	支持少量 NO MOQ	品种齐全 In Full Range